2836

Resp. w/Aff. #7 T. Bell. 6·26·03

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In Re: Application Ser. No. 09/886,437 : Art Unit 2836

Filed 6/21/01 : Exr. ZEEV KITOV

Inventors Cohen et al : Atty Dkt No YOR920000772US1

For:INTEGRATED CIRCUIT OVER VOLTAGE PROTECTION
Response to 3/13/03 Office Action

Commissioner for Patents
P.O.Box 1450
Alexandria, Va.22313-1450

Sir:

In response to the 3/13/03 Office Action in which there are a Drawing section, an Objection section and a claim rejection section:

With respect to the objection to the drawing section: an enclosed two sheet set of informal drawings assembled to address examiner's objections are provided for replacement with the examiner's approval. Approval is asked.

With respect to the objection section :

Reconsideration of the point in enumerated paragraph 3 concerning a believed to be "a nondestructive unlimited current". is respectfully requested for the reason that what is being described on lines 9 and 10 of claim 1 and line 10 of claim 9, is the current at "A" of Fig. 2 with a breakdown type flow not shown beyond the scale of Fig.2. With respect to the point concerning "unimpeded " in lines 14 and 16 on page 4 that terminology if on reconsideration is considered confusing can be removed. With respect to the point on claim 14 one way to look at it

is that the thickness is such that a connection is only made at a node where passing of the overvoltage is desired.

With respect to the claim rejections sections:

It is respectfully requested that the 35USC103 rejections be reconsidered for the following general reasons. The standard over voltage protection techniques used in the art encounter large fields in the densly packed integrated circuits. This invention teaches how to shunt over voltages at nodes in those densely packed structures by providing a structure of selected thickness and material at any critical node. The application of the standard techniques in the art as represented by the Zandman and the note 9307 references do not teach how to handle the conditions developing in the art as described on page 2 of the specification. It is unclear how the Zandman formula (page 250) could be applied in the nanometer thickness ranges such as to support an assertion of applicability to any thickness. Similarly the art in those dimensions is not such that the Pryor reference, relied on in the rejections for structural dimensions of the order of 100 nanometers, would come to the mind of one skillled in the art trying to solve the type of problem in the invention. The method of making, where planar processes are involved, is seldom inherent in the structure.

In view of the above, it is respectfully urged that applicants' invention is solving a need in the integrated circuit art where fields of several Millionvolts per Centimeter are encountered by providing an element that is connected into a critical node in the circuitry that shunts spikes and surges to ground and the art of record neither teaches nor suggests it.

Respectfully submitted,

Alvin J Riddles 6/13/03

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